WHAT IS CLAIMED IS:

1. A semiconductor memory device, having a storage node contact hole aligned at bit line spacers formed at both side walls of a bit line stack and exposing a pad, the device comprising a multi-layered storage node contact plug formed in the storage node contact hole, the mulit-layered storage node contact plug having a first storage node contact plug and a second storage node contact plug formed on the first storage node contact plug.

2. The semiconductor memory device of claim 1, wherein the first storage node contact plug is formed of a titanium nitride layer and the second storage node contact plug is formed of a polysilicon layer.

3. The semiconductor memory device of claim 1, further comprising an ohmic layer formed on the pad and under the first storage node contact plug.

4. The semiconductor memory device of claim 3, wherein the ohmic layer is formed of one of the group consisting of titanium (Ti), cobalt (Co), molybdenum (Mo) and tungsten (W).

5. The semiconductor memory device of claim 1, further comprising a barrier metal layer formed on the second storage node contact plug, wherein the barrier metal layer functions as a third storage node contact plug.

6. The semiconductor memory device of claim 5, wherein the barrier metal layer

is formed of one of a titanium nitride layer and a tantalum nitride layer.

7. The semiconductor memory device of claim 1, wherein the pad is formed of a polysilicon layer.

8. The semiconductor memory device of claim 1, wherein the second storage node contact plug has a thickness greater than a thickness of the first storage node contact plug.

9. A semiconductor memory device, comprising:

a pad formed on a semiconductor substrate;

an interlayer dielectric layer formed on the pad and substrate to insulate the pad;

a bit line stack formed on the interlayer dielectric layer;

a pair of bit line spacers formed at both side walls of the bit line stack;

a storage node contact hole, formed within the interlayer dielectric layer, exposing the pad and aligned between the bit line spacers; and

a multi-layered storage node contact plug formed within the storage node contact hole, including a first storage node contact plug and a second storage node contact plug formed on the first storage node contact plug.

10. The semiconductor memory device of claim 9, wherein the first storage node contact plug is formed of a titanium nitride layer and the second storage node contact plug is formed of a polysilicon layer.

11. The semiconductor memory device of claim 9, wherein the bit line stack comprises a bit line barrier metal layer, a bit line conductive layer, and a bit line cap layer which are sequentialy deposited.

12. The semiconductor memory device of claim 11, wherein the bit line barrier metal layer is formed of a titanium nitride layer, the bit line conductive layer is formed of a tungsten layer, and the bit line cap layer is formed of a silicon nitride layer.

13. The semiconductor memory device of claim 9, further comprising a barrier metal layer formed on the second storage node contact plug.

14. A method for fabricating a semiconductor memory device comprising:

forming a pad on a semiconductor substrate;

forming an interlayer dielectric layer on the pad and semiconductor substrate for insulating the pad;

forming a bit line stack on the interlayer dielectric layer;

forming a pair of bit line spacers at both side walls of the bit line stack;

forming a storage node contact hole in the interlayer dielectric layer using a self align contact etching method, the storage node contact hole being aligned at the bit line spacers and exposing the pad; and

forming a multi-layered storage node contact plug in the storage node contact hole, by sequentially forming a first storage node contact plug and a second node contact plug in the storage node contact hole.

15. The method for fabricating a semiconductor memory device of claim 14, wherein the first storage node contact plug is formed of a titanium nitride layer and the second storage node contact plug is formed of a polysilicon layer.

16. The method for fabricating a semiconductor memory device of claim 14, further comprising forming a barrier metal layer on the second storage node contact plug, the barrier metal layer functioning as a third storage node contact plug.

17. The method for fabricating a semiconductor memory device of claim 16, wherein the barrier metal layer is formed of one of a titanium nitride layer and a tantalum nitride layer.

18. The method for fabricating a semiconductor memory device of claim 16, wherein the forming of the multi-layered storage node contact plug comprises:

forming a first storage node contact plug material layer on an entire surface of the semiconductor substrate after the storage node contact hole is formed, thereby partially filling the storage node contact hole;

forming a second storage node contact plug material layer on the first storage node contact plug material layer to sufficiently fill the storage node contact hole;

forming a second storage node contact plug in the storage node contact hole by etching back the second storage node contact plug material layer;

forming a barrier metal material layer on the entire surface of the semiconductor substrate on which the second storage node contact plug is formed; and

etching the first storage node contact plug material layer and the barrier metal material layer on the bit line stack.

19. The method for fabricating a semiconductor memory device of claim 14, further comprising forming an ohmic layer on the pad and under the first storage node contact plug.

20. The method for fabricating a semiconductor memory device of claim 19, wherein the ohmic layer is formed of one selected from the group consisting of titanium (Ti), cobalt (Co), molybdenum (Mo) and tungsten (W).